This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently amended) A monolithic structure, comprising:

~~a semiconductor substrate having a first surface;~~

~~one or more~~ a first lateral device having a first source terminal, a first drain terminal, and a first gate terminal[[;]], each of said first source, first drain, and first gate terminals terminating on [[said]]a first surface of a semiconductor substrate; and

~~one or more~~ a second lateral device having a second source terminal, a second drain terminal and a second gate terminal[[;]], each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate[[; and;]],

wherein said ~~one or more~~ first lateral device [[being]]is combined with said ~~one or more~~ second lateral ~~power transistor~~ device on said substrate, said first source terminal is connected to said second source terminal to define a common source terminal of the monolithic structure, and a first electrically isolated lead comprises the common source terminal.

2. (Cancelled)

3. (Currently amended) The monolithic structure of claim [[2]]1 further comprising ~~at least one~~ a second electrically isolated lead comprising said first drain terminal and a third electrically isolated lead[[s]] comprising said ~~first and~~ second drain terminal[[s;]], wherein said first and second drain terminals [[being]]are

electrically independent of each other.

4. (Currently amended) The monolithic structure of claim 3 further comprising ~~at least one third and~~ a fourth electrically isolated lead[[s]] comprising said first gate terminal and a fifth electrically isolated lead comprising said second gate terminals~~; wherein~~ ,said first and second gate terminals being electrically independent of each other.

5. (Currently amended) The monolithic structure of claim 3 wherein said first gate terminal [[being]]is connected to said second drain terminal[[;]]and said second gate terminal [[being]]is connected to said first drain terminal.

6. (Currently amended) The monolithic structure of claim 1 wherein each of said first and second lateral devices [[is]]comprises a lateral power MOSFET.

7. (Currently amended) A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said monolithic structure comprising[[;]]:

~~semiconductor substrate having a first surface;~~

a first lateral power transistor device ~~having~~comprising a first source terminal, a first drain terminal and a first gate terminal[[;]], each of said first source, first drain, and first gate terminals terminating on [[said]] a first surface of the semiconductor substrate;

a second lateral power transistor device ~~having~~comprising a second source terminal, a second drain terminal, and a second gate terminal[[;]], each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate[[;]], said first gate terminal being connected to said second drain terminal[[;]], said second gate terminal being connected to said first drain terminal[[;]], and said first and second drain terminals being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal [[being]] connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal; and

a third electrically isolated lead comprising said second drain terminal.

8. (Currently amended) The monolithic structure of claim 7 wherein each of said first and second lateral power transistor devices [[is]]comprises a lateral power MOSFET.

9. (Currently amended) A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said structure comprising[[;]]:

~~a semiconductor substrate having a first surface;~~

a first lateral power transistor device ~~having~~comprising a first source terminal, a first drain terminal, and a first gate terminal[[;]], each of said first source, first drain, and first gate terminals terminating on [[said]]a first surface of the semiconductor substrate;

a second lateral power transistor device ~~having~~comprising a second source terminal, a second drain terminal, and a second gate terminal[[;]], each of said second source, second drain, and second gate terminals terminating on said first surface[[;]], said first and second drain terminals being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal [[being]] connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal;

a third electrically isolated lead comprising said second drain terminal; and

a fourth electrically isolated lead comprising said first gate terminal [[being]] connected to said second gate terminal.

10. (Currently amended) The monolithic structure of claim 9 wherein each of said first and second lateral power transistor devices [[is]]comprises a lateral power MOSFET.

11. (Currently amended) The monolithic structure of claim 9 wherein a size of said second lateral power transistor is [[of]] substantially smaller [[size]] than a size of said first lateral power transistor.

12. (Currently amended) The monolithic structure of claim 9 wherein a first threshold voltage of said first lateral power transistor is substantially different from a second threshold voltage of [[and]] said second lateral power transistors ~~each have substantially different threshold voltages; said~~ and a difference in said first and second threshold voltages is at least ~~ranging from~~ approximately 0.1 V ~~and greater~~.

13. (Currently amended) A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said structure comprising[[;]]:

~~a semiconductor substrate having a first surface;~~

a first lateral power transistor device ~~having~~comprising a first source terminal, a first drain terminal, and a first gate terminal[[;]], said first source, first drain, and first gate terminals terminating on [[said]]a first surface of the semiconductor substrate;

a second lateral power transistor device having a second source terminal[[;]], a second drain terminal, and a second gate terminal[[;]], said second source, second drain,

and second gate terminals terminating on said first surface[[;]], said first and second gate terminals being electrically independent of each other; and[[;]] said first and second drain terminal being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal [[being]] connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal;

a third electrically isolated lead comprising said second drain terminal;

a fourth electrically isolated lead comprising said first gate terminal; and

a fifth electrically isolated lead comprising said second gate terminal.

14. (Currently amended) The monolithic structure of claim 13 wherein each of said first and second lateral power transistor devices [[is]]comprises a lateral power MOSFET.

15. (Currently amended) The monolithic structure of claim 13 wherein a size of said second lateral power transistor is [[of]] substantially smaller [[size]] than a size of said first lateral power transistor.

16. (Currently amended) The monolithic structure of claim 13 wherein a first threshold voltage of said first lateral power transistor is substantially different from a second threshold voltage of [[and]]said second lateral power transistors ~~each have substantially different threshold voltages; said~~, and a difference in threshold voltages is at least ~~ranging from~~ approximately 0.1 V ~~and greater~~.